Abstract
In this paper a clock gated 8B/10B encoder and 10B/8B decoder circuit is implemented. In this we design the encoder decoder circuit with gated clock as it optimized the power without degrading the performance of the circuits. The technology used in this paper is gated clock circuit using negative latch. This gated clock then used to control the encoder and decoder circuit. The RTL view of encoder and decoder with clock gating are shown in Figures 13 and 14. Encoder without clock gating circuit at 20 MHz consumes hierarchy power and on-chip power is 0.10 mW and 111 mW respectively and at 200 MHz consumes hierarchy power and on-chip power is 1.05 mW and 149 mW respectively. Encoder with clock gating circuit at 20 MHz consumes hierarchy power and on-chip power is 0.05 mW and 108 mW respectively and at 200 MHz consumes hierarchy power and on-chip power is 0.47 mW and 113 mW respectively. Decoder without clock gating circuit at 20 MHz consumes hierarchy power and on-chip power is 0.05 mW and 108 mW respectively and at 200 MHz consumes hierarchy power and on-chip power is 0.49 mW and 116 mW respectively. Decoder with clock gating circuit at 20 MHz consumes hierarchy power and on-chip power is 0.05 mW and 108 mW respectively and at 200 MHz consumes hierarchy power and on-chip power is 0.49 mW and 113 mW respectively. The encoder and decoder circuits are design using verilog HDL and are simulated in ModelSim 10.3c. For the RTL view and power report of the implemented circuit we used Xilinx ISE suite 13.4.

I. INTRODUCTION

In today’s time the VLSI industry is growing rapidly and it demands for the devices which consume less power and there is no impact on their performance. Maintaining the performance with less power consumption is the big task for the engineers. Therefore, the maximum time is spent on the power reduction without affecting the performance by the VLSI engineers. There are many techniques used to reduce the power consumption of the design.

Clock Gating is a technique used for reduction of power in the digital design by clock net. In clock gating technique the clock is disabled at the situation where it is not necessary, thus this reduces the power consumption. Clock gating simply switch off the clock where it is unnecessarily consumes power. By doing this the power consumption is less without affecting the performance of the design.

There are various techniques used for clock gating as: NAND gate, AND gate, latch based AND/NOR gate clock gating, multiplexer based clock gating. The latest technique for clock gating generation is using of negative/positive latch.

In this paper, we have designed the 8B/10B encoder and decoder with clock gating. This reduces the power consumption of the encoder and decoder circuit. 8B/10B encoder and 10B/8B decoder are widely used because of their low transmission rate and DC compensation feature. They are used in various employments such as PCI express, USB 3.0, gigabit ethernet and many more.

In this paper, Section II illustrate the clock gating technique which is used in this paper, Section III illustrate the architecture of encoder and decoder using clock gating technique discussed in Section II, Section VI shows the simulation results and Section V describes the conclusion.

II. CLOCK GATING TECHNIQUE USING NEGATIVE LATCH

The recent clock gating technique which is used in this paper for generating the gated clock is using negative latch circuit. When the target device’s clock is off then the